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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,891	12/19/2001	Gee Sung Chae	8733.495.00	8845

30827 7590 10/03/2002

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EXAMINER
DUONG, THOI V

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,891	CHAE, GEE SUNG	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujikawa et al. (USPN 6,445,428 B1).

As shown in Fig. 4, Fujikawa discloses a liquid crystal display (LCD) device comprising:

a thin film transistor (TFT) 30 having a source electrode 27b, a drain electrode 27e, and a gate electrode 22 within a pixel region defined by a plurality of gate lines and data lines (see Fig. 2), the source and drain electrodes having a low resistance material including aluminum (Al) (col. 8, lines 11-25);

an ohmic contact layer 26A, 26B on the active region; and

a buffer layer 27a, 27d on the ohmic contact layer;

wherein the source and drain electrodes are on the buffer layer,

wherein the gate electrode includes a low resistance material including aluminum (Al) (col. 9, lines 8-10);

wherein the buffer layer includes a metal, titanium (Ti) (col. 8, lines 11-25);

The LCD device further comprises:

a gate insulating film 23 on an entire surface including the gate electrode, wherein the gate insulating film includes silicon nitride film (col. 10, lines 38-40);

a transparent pixel electrode of ITO electrically connected with the buffer layer (col. 8, lines 47-51).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa et al. (USPN 6,445,428 B1) in view of Applicant's Prior Art (Figs. 2A-2E).

As shown in Figs. 5A-5E, Fujikawa discloses a method of fabricating a TFT comprising:

forming a gate electrode 22 on a substrate 21;

forming a gate insulating film 23, a semiconductor layer 24, an ohmic contact layer 26A, 26B, and a buffer layer 27a, 27d on the gate electrode;

forming a pixel electrode on the buffer layer;

forming source and drain electrodes 27b, 27e on the buffer layer; and

forming a passivation layer 28 on a surface of the substrate,

wherein the gate electrode includes aluminum (Al) (col. 9, lines 8-10),

wherein the buffer layer includes titanium (Ti) (col. 8, lines 11-25),

wherein the source and drain electrodes include aluminum (Al) (col. 8, lines 11-25),

wherein the pixel electrode includes indium tin oxide (col. 8, lines 47-51),

wherein the drain electrode is electrically connected with the pixel electrode,

wherein the gate electrode is deposited by a sputtering process (col. 9, lines 8-10),

wherein the gate electrode is patterned using photolithography (col. 10, lines 55-59),

wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are formed on the gate insulating film by a plasma enhanced chemical vapor deposition (PECVD) process, wherein the semiconductor layer, the ohmic contact layer, and the buffer layer are patterned (col. 9, lines 15-32),

wherein the pixel electrode is formed by a sputtering process, wherein the pixel electrode is patterned (col. 9, lines 60-67), and

wherein the passivation layer is formed by a deposition process (col. 9, lines 54-59).

Fujikawa discloses all aspects of the instant invention as shown above except for forming the passivation layer on the pixel electrode and a common electrode on the passivation layer. Applican't Prior Art (Figs. 2A-2E) discloses a method for manufacturing an in-plane switching mode liquid crystal display (LCD) device comprising forming a pixel electrode on a drain electrode 207 and forming a transparent

common electrode on a passivation layer 209. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Fujikawa with the teaching of Applicant's Prior Art by forming the pixel electrode on the drain electrode formed on the buffer layer, the passivation layer on the pixel electrode, and a common electrode on the passivation layer so as to complete the fabrication of a TFT without forming a contact hole through the passivation layer.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

Thoi Duong

09/24/2002

William L. Sikes
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